

What is claimed is:

1. A semiconductor memory device having sense amplifier array blocks between neighboring unit memory cell array blocks  
5 in a column direction, the semiconductor memory device comprising:

a first sense amplifier driving line configured by passing the sense amplifiers in a row direction;

10 a second sense amplifier driving line configured by passing the sense amplifiers in a row direction;

a plurality of first NMOS transistors, which are disposed in the sense amplifier array block, for locally performing a pull-up operation of the first sense amplifier driving line in response to a first control signal; and

15 a second NMOS transistor, which is disposed in a hole area, for performing a pull-down operation of the second sense amplifier driving line in response to a second control signal.

2. The semiconductor memory device as recited in claim 1,  
20 wherein the second NMOS transistor has a relatively large size to have a drivability to perform the pull-down operation of the second sense amplifier driving line against a resistance of the second amplifier driving line, and a size of the first NMOS transistor is smaller than that of the second NMOS  
25 transistor.

3. The semiconductor memory device as recited in claim 2,

further comprising a third NMOS transistor, which is disposed in the hole area, for performing the pull-up operation of the first sense amplifier driving line in the response to the first control signal.

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4. The semiconductor memory device as recited in claim 3, wherein the third NMOS transistor has a smaller size than the second NMOS transistor.

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5. The semiconductor memory device as recited in claim 1, wherein each first NMOS transistor is disposed for a set of two sense amplifiers in the sense amplifier array block.

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6. The semiconductor memory device as recited in claim 1, wherein a gate extension direction of transistors configuring the sense amplifiers is substantially perpendicular to a gate extension direction of the first NMOS transistors.

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7. A semiconductor memory device having sense amplifier array blocks between neighboring unit memory cell array blocks in a column direction, the semiconductor memory device comprising:

a first sense amplifier driving line configured by passing the sense amplifiers in a row direction;

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a second sense amplifier driving line configured by passing the sense amplifiers in a row direction;

a plurality of first NMOS transistors, which is disposed

in the sense amplifier array block, for locally performing a pull-up operation of the first sense amplifier driving line in response to a first control signal; and

5 a plurality of second NMOS transistors, which is disposed in the sense amplifier array block, for locally performing a pull-down operation of the second sense amplifier driving line in response to a second control signal.

8. The semiconductor memory device as recited in claim 7,  
10 further comprising a third NMOS transistor, which is disposed in the hole area, for performing the pull-up operation of the first sense amplifier driving line in the response to the first control signal.

15 9. The semiconductor memory device as recited in claim 8, further comprising a fourth NMOS transistor, which is disposed in the hole area, for performing the pull-down operation of the second sense amplifier driving line in the response to the second control signal.

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10. The semiconductor memory device as recited in claim 9, wherein the third and fourth NMOS transistor have a smaller size than the first and second NMOS transistor, respectively.

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11. The semiconductor memory device as recited in claim 9, wherein one first NMOS transistor and one second NMOS transistor are disposed for a set of two sense amplifier in

the sense amplifier array block.

12. The semiconductor memory device as recited in claim  
7, wherein a gate extension direction of transistors  
5 configuring the sense amplifiers is substantially  
perpendicular to a gate extension direction of the first and  
second NMOS transistors.